WHAT IS CLAIMED IS:

1. A cascaded interpolator configured to receive a one-bit

2 input signal, comprising:

3 a multiple order interpolation filter, configured to generate

4 a sample range from at least three input samples associated with

5 said one-bit input signal; and

6 a linear interpolation filter, associated with said multiple

7 order interpolation filter, configured to develop a plurality of

8 samples within said sample range.

2. The interpolator as recited in Claim 1 wherein said

multiple order interpolation filter is configured to generate said

sample range from four input samples associated with said one-bit

input signal.

3. The interpolator as recited in Claim 1 wherein said

2 sample range is a subset of a range associated with said input

3 samples.

4. The interpolator as recited in Claim 1 wherein said

2 multiple order interpolation filter is a finite impulse response

3 filter.

5. The interpolator as recited in Claim 1 wherein said

2 linear interpolation filter is configured to generate 512 samples.

6.   A method of interpolating a one-bit input signal,

2   comprising:

3   generating a sample range from at least three input samples

4   associated with said one-bit input signal; and

5   developing a plurality of samples within said sample range.

7.   The method as recited in Claim 6 wherein said generating

2   comprises generating said sample range from four input samples

3   associated with said one-bit input signal.

8.   The method as recited in Claim 6 wherein said sample

range is a subset of a range associated with said input samples.

9.   The method as recited in Claim 6 wherein said generating

is performed by a multiple order interpolation filter and said

developing is performed by a linear interpolation filter.

10.   The method as recited in Claim 9 wherein said multiple

2   order interpolation filter is a finite impulse response filter.

11.   A resampler for use with a bit pump having a receive path couplable to an oscillator, comprising:

an interpolation stage, coupled to an input of said resampler, configured to receive a one-bit input signal representing at least a portion of a receive signal propagating along said receive path and including:

a multiple order interpolation filter configured to generate an intermediate sample range from at least three input samples associated with said one-bit input signal, and

a linear interpolation filter, associated with said multiple order interpolation filter, configured to develop a plurality of intermediate samples within said intermediate sample range; and

a selection stage, coupled to said interpolation stage, configured to select one of said plurality of intermediate samples thereby providing an output sample that corresponds to a phase of said oscillator.

12. The resampler as recited in Claim 11 wherein said interpolation stage is configured to receive multiple one-bit input signals representing at least a portion of said receive signal and said interpolation stage further comprises a plurality of linear interpolation filters configured to develop a plurality of intermediate samples from at least two input samples associated with ones of said multiple one-bit input signals.

13. The resampler as recited in Claim 12 wherein said selection stage is configured to select corresponding ones of said plurality of intermediate samples from said at least two input samples associated with ones of said multiple one-bit input signals thereby providing output samples that correspond to said phase of said oscillator.

14. The resampler as recited in Claim 13 further comprising a combining stage configured to combine said output samples.

15. The resampler as recited in Claim 11 further comprising a filter stage configured to filter said output sample.

16. The resampler as recited in Claim 15 wherein said filter stage comprises one of a second and third order section.

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17.   The resampler as recited in Claim 11 further comprising

2   a delay stage.

18.   The resampler as recited in Claim 11 wherein said

2   multiple order interpolation filter is configured to generate said

3   intermediate sample range from four input samples associated with

4   said one-bit input signal.

19.   The resampler as recited in Claim 11 wherein said

intermediate sample range is a subset of a range associated with

said input samples.

20.   The resampler as recited in Claim 11 wherein said

multiple order interpolation filter is a finite impulse response

filter.

21. A method of resampling at least a portion of a receive

2 signal propagating along a receive path couplable to an oscillator

3 of a bit pump, comprising:

4   receiving a one-bit input signal representing at least a

5 portion of said receive signal;

6   generating an intermediate sample range from at least three

7 input samples associated with said one-bit input signal;

8   developing a plurality of intermediate samples within said

9 intermediate sample range; and

10   selecting one of said plurality of intermediate samples

11 thereby providing an output sample that corresponds to a phase of

12 said oscillator.

22. The method as recited in Claim 21 further comprising

receiving multiple one-bit input signals representing at least a

portion of said receive signal and developing a plurality of

intermediate samples from at least two input samples associated

5 with ones of said multiple one-bit input signals.

23. The method as recited in Claim 22 further comprising
2 selecting corresponding ones of said plurality of intermediate
3 samples from said at least two input samples associated with ones
4 of said multiple one-bit input signals thereby providing output
5 samples that correspond to said phase of said oscillator.

24. The method as recited in Claim 23 further comprising
2 combining said output samples.

25. The method as recited in Claim 21 further comprising
filtering said output sample.

26. The method as recited in Claim 25 wherein said filtering
is performed by a filter stage having one of a second and third
order section.

27. The method as recited in Claim 22 further comprising
2 delaying ones of said multiple one-bit input signals.

28. The method as recited in Claim 21 wherein said generating
2 said intermediate sample range is from four input samples
3 associated with said one-bit input signal.

29. The method as recited in Claim 21 wherein said

2   intermediate sample range is a subset of a range associated with

3   said input samples.

30. The method as recited in Claim 21 wherein said generating

2   is performed by a multiple order finite impulse response

3   interpolation filter.

31. A bit pump having a transmit and receive path,

2 comprising:

3   a precoder, coupled to said transmit path, that preconditions

4 a transmit signal propagating along said transmit path;

5   a modulator, coupled to said precoder, that reduces a noise

6 associated with said transmit signal;

7   an analog-to-digital converter, coupled to said receive path,

8 that converts a receive signal received at said bit pump into a

9 digital format;

10   a resampler, coupled to said analog-to-digital converter and

11 an oscillator of said bit pump, including:

12   an interpolation stage, coupled to an input of said

13   resampler, that receives a one-bit input signal representing

14   at least a portion of said receive signal, including:

15   a multiple order interpolation filter that generates

16   an intermediate sample range from at least three input

17   samples associated with said one-bit input signal, and

18   a linear interpolation filter, associated with said

19   multiple order interpolation filter, that develops a

20   plurality   of   intermediate   samples   within   said

21   intermediate sample range, and

22   a selection stage, coupled to said interpolation stage,

23   that selects one of said plurality of intermediate samples

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24   thereby providing an output sample that corresponds to a phase

25   of said oscillator; and

26   an echo canceling system, coupled between said transmit and

27   receive path, that attenuates an echo in said receive signal.

32. The bit pump as recited in Claim 31 wherein said

2   interpolation stage receives multiple one-bit input signals

3   representing at least a portion of said receive signal and said

4   interpolation stage further comprises a plurality of linear

5   interpolation filters that develop a plurality of intermediate

6   samples from at least two input samples associated with ones of

7   said multiple one-bit input signals.

33. The bit pump as recited in Claim 32 wherein said

2   selection stage selects corresponding ones of said plurality of

3   intermediate samples from said at least two input samples

4   associated with ones of said multiple one-bit input signals thereby

5   providing output samples that correspond to said phase of said

6   oscillator.

34. The bit pump as recited in Claim 33 wherein said

2   resampler further comprises a combining stage that combines said

3   output samples.

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35. The bit pump as recited in Claim 31 wherein said resampler further comprises a filter stage that filters said output sample.

36. The bit pump as recited in Claim 35 wherein said filter stage comprises one of a second and third order section.

37. The bit pump as recited in Claim 31 wherein said resampler further comprises a delay stage.

38. The bit pump as recited in Claim 31 wherein said multiple order interpolation filter generates said intermediate sample range from four input samples associated with said one-bit input signal.

39. The bit pump as recited in Claim 31 wherein said intermediate sample range is a subset of a range associated with said input samples.

40. The bit pump as recited in Claim 31 wherein said multiple order interpolation filter is a finite impulse response filter.

41. A transceiver, comprising:

2   a framer that formats signals within said transceiver;

3   a bit pump coupled to said framer and having a transmit and

4   receive path, including:

5   a precoder, coupled to said transmit path, that

6   preconditions a transmit signal propagating along said

7   transmit path;

8   a modulator, coupled to said precoder, that reduces a

9   noise associated with said transmit signal;

10   an analog-to-digital converter, coupled to said receive

11 path, that converts a receive signal received at said bit pump

12 into a digital format;

13   a resampler, coupled to said analog-to-digital converter

14 and an oscillator of said bit pump, including:

15   an interpolation stage, coupled to an input of said

16 resampler, that receives a one-bit input signal

17 representing at least a portion of said receive signal,

18   including:

19   a multiple order interpolation filter that

20   generates an intermediate sample range from at

21   least three input samples associated with said one-

22   bit input signal, and

23   a linear interpolation filter, associated with

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24   said multiple order interpolation filter, that

25   develops a plurality of intermediate samples within

26   said intermediate sample range, and

27   a selection stage, coupled to said interpolation

28   stage, that selects one of said plurality of intermediate

29   samples thereby providing an output sample that

30   corresponds to a phase of said oscillator; and

31   an echo canceling system, coupled between said transmit

32   and receive path, that attenuates an echo in said receive

33 signal; and

34 a controller that controls an operation of said framer and

35 said bit pump.

42. The transceiver as recited in Claim 41 wherein said

interpolation stage receives multiple one-bit input signals

representing at least a portion of said receive signal and said

interpolation stage further comprises a plurality of linear

interpolation filters that develop a plurality of intermediate

samples from at least two input samples associated with ones of

said multiple one-bit input signals.

43.   The transceiver as recited in Claim 42 wherein said

2   selection stage selects corresponding ones of said plurality of

3   intermediate samples from said at least two input samples

4   associated with ones of said multiple one-bit input signals thereby

5   providing output samples that correspond to said phase of said

6   oscillator.

44.   The transceiver as recited in Claim 43 wherein said

2   resampler further comprises a combining stage that combines said

3   output samples.

45.   The transceiver as recited in Claim 41 wherein said

2   resampler further comprises a filter stage that filters said output

3   sample.

46.   The transceiver as recited in Claim 45 wherein said

2   filter stage comprises one of a second and third order section.

47.   The transceiver as recited in Claim 41 wherein said

2   resampler further comprises a delay stage.

48. The transceiver as recited in Claim 41 wherein said

2   multiple order interpolation filter generates said intermediate

3   sample range from four input samples associated with said one-bit

4   input signal.

49. The transceiver as recited in Claim 41 wherein said

2   intermediate sample range is a subset of a range associated with

3   said input samples.

50. The transceiver as recited in Claim 41 wherein said

multiple order interpolation filter is a finite impulse response

filter.